ABSTRACT OF THE DISCLOSURE

A circuit and method are disclosed for a memory device, such as a phase change memory. Specifically, there is disclosed a memory having a plurality of columns of memory cells, with each column of memory cells being coupled to a bit or data line. Each memory cell includes a programmable resistive element coupled in series with a select transistor. Each bit line is coupled to a distinct reference cell and a distinct transistor. The transistor is coupled between the corresponding bit line and a reference voltage, such as ground. During a memory read operation, the transistor, reference cell and addressed memory cell form a differential amplifier circuit. The output of the differential amplifier circuit is coupled to the data output terminals of the phase change memory.